23.1 A Broadband Receive Chain in 65nm CMOS

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Receiver front-end solutions capable of covering a wide range of frequencies could be employed in several interesting applications, such as multi-band reception, future software-defined radios and other emerging broadband applications, e.g., MB-OFDM UWB [1]. To avoid multiple dedicated front-ends for multi-band reception, a wideband front-end with the ability to receive multiple bands is required. In this paper, a fully integrated broadband receiver front-end in 65nm CMOS is described. A highly linear low-noise low-power receiver covering a spectrum from 2 to 8GHz is demonstrated. The proposed topology inherently provides single-ended input to differential output conversion, thereby obviating the requirement of an external balun.

The receiver block diagram is shown in Fig. 23.1.1. The RF front-end part consists of a single-ended input wideband LNA which drives, in differential mode, an active mixer. A transimpedance amplifier (TIA) with 1st-order baseband filtering follows the mixer. This configuration is essentially targeted for direct conversion. A dedicated LO driver to generate an appropriate LO signal is included on the chip.

To achieve linear broadband low-noise operation, the LNA uses a cascode configuration with dual loop feedback, of which one loop incorporates an integrated transformer. The LNA topology is shown in Fig. 23.1.2. By using a transformer, broadband operation can inherently be achieved while maintaining low noise [2]. Compared to plain inductive degeneration or LC-ladder-based broadband LNAs [3], the occupied area is significantly reduced, since the primary and secondary inductors can be stacked. Additionally, the required inductor values can be reduced due to the desired presence of mutual magnetic coupling. In this work a transformer is used which also acts as a balun. The primary coil at the output of the LNA consists of 8 windings with multiple taps, distributed over 5 metal layers with an inductance value of 9nH, while occupying a relatively small area of 120×130μm^2. This tapped transformer structure allows the LNA to accommodate a single-ended input and a differential output, avoiding the necessity of an external wideband balun. The secondary coil consists of one single turn on stacked top metal layers with an inductance value of 240pH. This transformer construction makes optimal use of the available metal layers to merge multiple functions in the transformer while keeping its size compact. A 3D view of the transformer is shown in the lower part of Fig. 23.1.2. Measurement of a separate LNA shows a noise figure (NF) of 2.5dB, a voltage gain of 12dB, and an IIP3 of +12dBm.

Since voltage headroom is limited in deep submicron technologies, a switched transconductance mixer [4] is chosen. As compared to other active mixer structures such as Gilbert mixers, this topology has the advantage of better compatibility with low supply voltage. In addition, in contrast with passive mixers, it provides gain. Another characteristic of this mixer topology is that it inherently converts the LNA output voltage into a current, thereby eliminating the need for intermediate transconductance stages or conversion resistors. The mixer structure is shown in Fig. 23.1.3. Current sources on top of the mixer core provide the bias currents and a control loop sets the common-mode levels. The switches at the LO port are based on inverters. The mixer transistor dimensions are chosen by considering the trade-off between noise and power consumption.

The LO driver consists of three push-pull stages, forming together one inverter (see Fig. 23.1.4). A properly biased push-pull topology gives more transconductance (g_m) at approximately the same capacitance compared to an inverter topology. Consequently, more gain and a larger bandwidth can be obtained. To avoid the need for capacitors to realize AC coupling between the stages and hence to save die area, each stage is duplicated. One section of each stage has a common-mode voltage around 0.3V and drives a PMOS device; the other section drives an NMOS device at 0.8V DC voltage. In the last section, the output nodes of each section are connected together and fed back to the input node of the first stage, realizing a common-mode voltage of 0.6V. This compound structure has a voltage gain of 5.4 maintained up to 8GHz while loaded by the mixer. One single-ended input/output LO buffer draws 5mA from a 1.2V supply.

The TIA comprises a 3-stage opamp with a parallel RC feedback network. The cut-off frequency is set to 264MHz as this high bandwidth is required for the MB-OFDM UWB standard, which is chosen as the application in this particular case. The first stage of the opamp is biased in subthreshold mode to minimize thermal noise at low bias currents. For a given g_m, which is determined by the thermal noise requirement, the devices have to be larger when they operate in the subthreshold regime, which also reduces their 1/*f* noise contribution. The opamp has a unity gain bandwidth of approximately 4GHz at low currents, indicating the benefits of a modern high-f_t technology. It achieves an open-loop voltage gain of 58dB.

The receiver chip is fabricated in a baseline 65nm CMOS technology with 8 metal layers. A chip micrograph is shown in Fig. 23.1.6. The chip area is 0.48mm^2, and its active area is less than 0.1mm^2. The receiver is characterized with on-wafer measurements. Figure 23.1.5 shows the measured receiver voltage gain over a range from 2.5 to 11GHz. The measured receiver noise figure is also shown in this figure. A gain of 23dB is achieved over a wide frequency range with a 3dB frequency at 8GHz. A receiver NF of 4.5dB is measured with the LO at 4GHz, which is competitive with [5] and [6]. With the LO at 7GHz the NF degrades by less than 1dB. A two-tone test (tones at 5GHz and 6.05GHz with the LO at 4GHz) shows an IIP3 of –7dBm. With two tones at 2.4GHz and 2.45GHz and the LO at 4.8GHz, the IIP2 is measured to be +18dBm. Of course, it is different for cases where the intermodulation product is not in the RF band. For instance, the 50MHz difference frequency for an input combination of 2.4 and 2.45GHz will only be seen by direct feedthrough from the RF port to baseband output through the mixer, which is suppressed. For that case, which is of importance for narrowband systems, even higher IIP2 values are observed. Altogether this shows that a linear receiver in deep submicron with low voltage headroom is still possible.

The complete receive chain operates from a 1.2V supply and draws an average current of 32.5mA (39mW), of which 15mA is for the LNA, 8.2mA is for the mixer plus LO switch and 9.3mA is for the TIA. The LO driver consumes an additional 10mA at an LO frequency of 8GHz. A summary of the measured key parameters is shown in Fig. 23.1.7.

References:

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[4] E.A.M. Klumperink, S.M. Louwsma, G.J.M. Wienk, and B. Nauta, "A CMOS Switched Transconductor Mixer," *IEEE J. Solid-State Circuits*, vol. 39, pp.1231-1240, Aug., 2004.

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[6] M. Ranjan and L. Larson, "A Sub-1mm^2 Dynamically Tuned CMOS MB-OFDM 3-to-8GHz UWB Receiver Front-End," *ISSCC Dig. Tech. Papers*, pp.128-129, Feb., 2006.

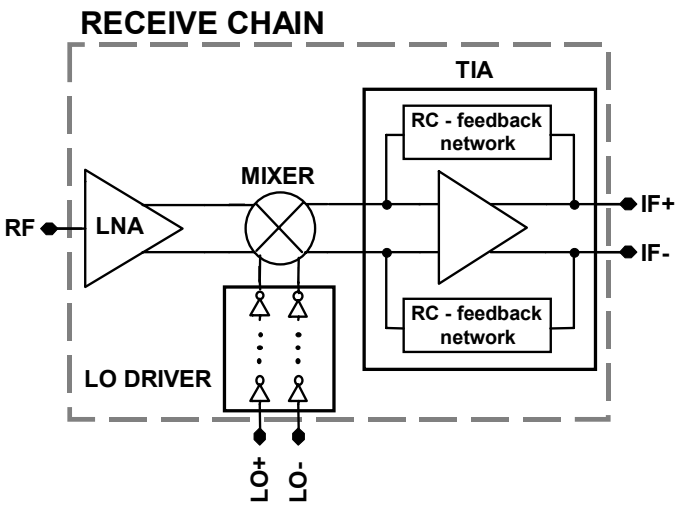

Figure 23.1.1: Block diagram of the broadband receiver chain.

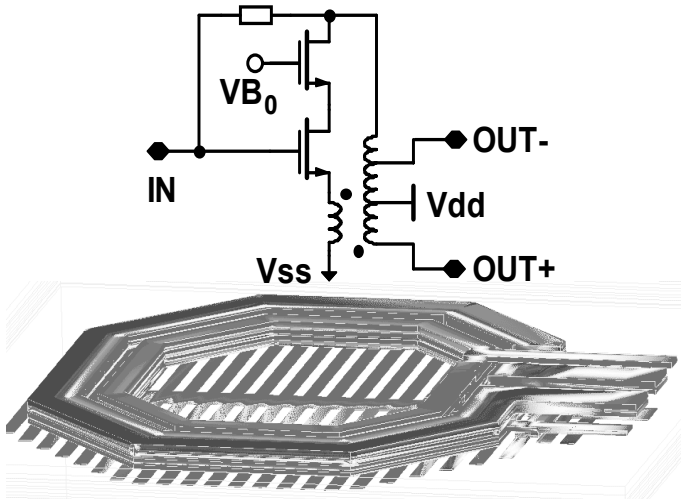

Figure 23.1.2: Double loop feedback LNA (biasing not shown) and 3D view of the transformer structure.

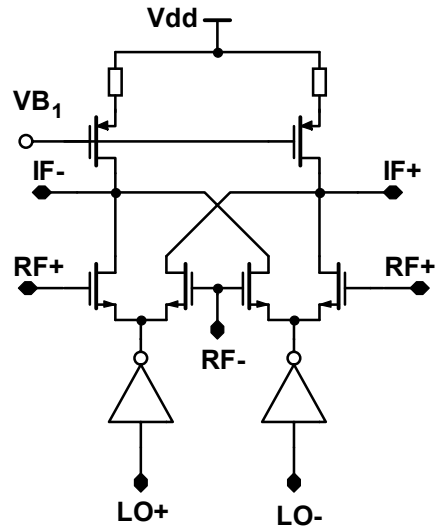

Figure 23.1.3: Circuit diagram of the switched transconductance mixer (biasing not shown).

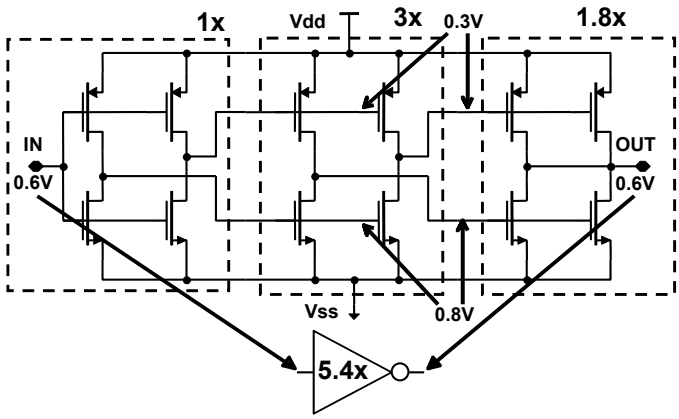

Figure 23.1.4: Push-pull LO driver stage.

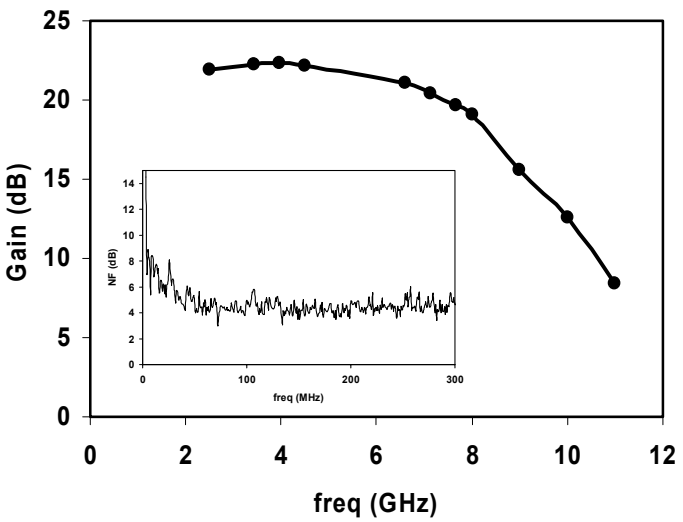

Figure 23.1.5: Measured receiver voltage gain and NF.

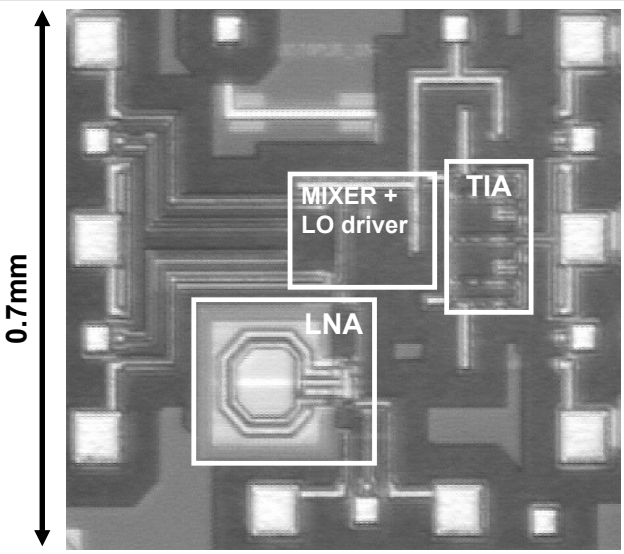

Figure 23.1.6: Chip micrograph.

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Parameter	*Value*
RX Gain	23dB
RX Bandwidth	2 to 8GHz
NF	4.5dB
IIP3	−7dBm
IIP2	+18dBm
S_{11}	−8dB
Power Dissipation	51mW@1.2V
Active Area	0.09mm^2
Technology	65nm CMOS

Figure 23.1.7: Measured performance of the receiver front-end.

